IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of		)	Art Unit:
	Knol, et al.	)	Examiner: unknown
Serial No.:	10/792,164	)	Docket No: HDI-001
Filed:	3/3/2004	)	

For: SYSTEM FOR REPRESENTING THE LOGICAL AND PHYSICAL INFORMATION OF AN INTEGRATED CIRCUIT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§1.97-1.98, the undersigned would like to make the following prior art references of record in the above-identified patent application. The undersigned believes that some or all of these references may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 C.F.R. §1.56.

While this Information Disclosure Statement may contain material information pursuant to 37 C.F.R. §1.56, it is not intended to constitute an admission that any individual reference referred to herein is prior art to the invention disclosed and claimed in the above-identified patent application.

Each reference listed herein may be accompanied by an explanation of its relevance. While this explanation is believed to generally reflect the contents of the references which the

undersigned believes a reasonable examiner might consider relevant and material to the examination of the above-identified patent application, it is not intended that the examiner rely on the description as unfailingly accurate or complete. A copy of each reference is enclosed for the express purpose of providing the examiner with an opportunity to perform an independent evaluation to arrive at an independent assessment of its relevance and materiality, if any, to the claimed subject matter.

Cited Art with reference attached:

Hwang, US 6,408,422, filed 1/19/99 as a cip of parent filed 5/27/98: Teaches a method for remapping logic modules to resources of a programmable gate array. Addresses the problem of designing floor plans in the rising gate count environment of modern FPGAs. Suggests a hierarchy of logic blocks of increasing generality and teaches libraries of pre-developed logic blocks such as adders, multipliers, etc. Use of logic blocks reduces design cycles and reduces design costs but it usually results in suboptimal performance. Therefore, use of predefined logic blocks conflicts with the objectives of optimizing performance. The invention is to remap logic blocks into resources of an FPGA.

Ginetti et al., US 6,170,080, filed 8/29/97: Teaches a system to design a floorplan of an integrated circuit at a high level of abstraction. The invention of this patent addresses the problems: 1) that the designer must synthesize the circuit design twice; 2) the designer must exchange large data files between several Electronic Design Automation Tools many times; 3) the designer must describe the circuit in a hardware description language before starting a floorplan of the circuit design. As such, the convention process wastes time and resources. The need addressed therefore is to provide a system for a designer to floorplan at a higher level of abstraction so the floorplan can be started before the netlist is finished. This allows such things as estimating inter-block wiring capacitance and wire load models can be estimated before circuit design is complete for good synthesis and optimization of the circuit design. However, a netlist must be completed before the floorplan can be completed. The tool taught can read and represent a logical netlists at a high level of abstraction and which can do logic block placement in the floorplan at a high level of abstraction. This tool allows breaking down a logical hierarchy to build a physical hierarchy or floorplan. The tool can also derive wire load models, extract inter-block capacitance values and communicate them to a synthesis tool

Moore et al., US 5,513,119, filed 6/21/95, continuation of a parent filed 8/10/93: Teaches a method to hierarchically group logic cells to form groups to be placed in an IC gate layout. The system is suppled with input design files defining the IC to be laid out, the groups to be placed and I/O buffers to be placed on the edge of a chip. The system reads the design files to create a database used for placing desired I/O buffers and for hierarchically grouping the cells and placing the groups. The buffers and groups can be moved to any valid locations within the IC.

database used for placing desired I/O buffers and for hierarchically grouping the cells and placing the groups. The buffers and groups can be moved to any valid locations within the IC.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 4/28/04
(Date Of Deposit)

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FORM PTO-1449 (Rev. 2-32) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. HDI-001	SERIAL NO. 10/792,164
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT KNOL ET AL.	
(USE SEVERAL SHEETS IF NECESSARY)	FILING DATE 3/3/04	GROUP unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROP.
	A	6,408,422	5/27/98	HWANG	716	3	5/27/98
	B	6,170,080	8/29/97	GINETTI ET AL.	716	18	8/29/97
	C	513,119	8/10/93	MOORE ET AL.	364	491	8/10/93
	D						
	E						
	F						
	G						
	H						
	I						
	J						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUB. DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	K						X	
	L						X	
	M							
	N							
	O							
	P							
	Q							
	R							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL		
	S	
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EXAMINER | DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.